REMARKS

Objection Regarding Formulation

The Examiner has objected to claim 5, because of two definite articles in lines 11 and 16-17. Applicant has amended claim 5 to clarify the use of the definite articles.

35 U.S.C. § 103 Rejections

The Examiner has rejected claims 1-10 under 35 U.S.C. § 103(a) as being obvious over Agarwal in view of Katoh. Applicant submits that the claims are patentable over the cited references.

Katoh discloses a completely different invention which would not and could not be combined with the invention of Agarwal. First, Katoh does not use a continuous layer without recesses of memory material, even though Agarwal calls for it. And second, Katoh uses tunneling magneto-resistance elements (TMR) instead of a ferroelectric polymer layer. Because of using the different physical effect, Katoh has to solve another underlying problem which Agarwal does not appreciate.

Agarwal in FIG. 4 illustrates lower electrode structures 14, 16 and 18 (word lines), in FIG. 5 illustrates upper conductive structures 34, 36 and 38 (bit lines), and a polymer ferroelectric material 30 between the word lines and the bit lines. This

polymer-based ferroelectric layer is formed as a continuous layer without any recesses and gaps. Agarwal even discloses in paragraph [0005] shown on page 1, column 1 in Agarwal:

> *[0005] For example, the present inventors have recognized at least one problem in fabricating multi-layer memories using polymer-based ferroelectrics (ferroelectric polymers). Specifically, they recognized that conventional fabrication methods that deposit the ferroelectric polymer over metal structures separated by empty gaps creates hills and valleys in the deposited ferroelectric material. The changing thickness of the ferroelectric material is undesirable, because it not only causes cell-to-cell performance variations, but also produces too many defective cells and thus reduces manufacturing yield. Poor yield ultimately raises the cost of manufacturing these type memories. Moreover, as the number of layers in a multi-layer memory increases, the hills and valleys tend to become higher and deeper, exaggerating the thickness variations in the deposited ferroelectric material and further detracting from desired performance and yield.* [Emphasis added.]

Agarwal teaches away from forming a layer with gaps as, for example, forming a layer only between the intersections of word lines and bit lines as Katoh does.

Agarwal furthermore states in paragraph [0034] and [0032] shown on page 2, column 2 in Agarwal:

> *[0034] FIG. 3 shows that after forming gap-filling structures 22 and 24, the exemplary method entails formation of a polymer-based ferroelectric layer 30. More specifically, this polymer-based ferroelectric layer is formed to a thickness of 10-1000 nanometers. In the exemplary embodiment, polymer-based ferroelectric layer 30 has different characteristics than the gap-filling layer, more precisely polymer-based gap-filling structures 22 and 24. Specifically, unlike the polymer-based gap-filling structures 22 and 24, which is optimized for spin casting, polymer-based ferroelectric layer 30 is optimized for other properties, such as its ferroelectricity.*

[0032] In some embodiments that use an insulative polymer filler, the polymer includes a polymer-based ferroelectric material. (As used herein, the term "ferroelectric," indicates that a subject material, material composition, or material structure, exhibits a detectable spontaneous electrical polarization in response to appropriate electrical stimulus. Thus, the term without other express contextual modification or qualification generally encompasses elemental ferroelectric materials as well as combination and composite ferroelectric materials.) Exemplary ferroelectric polymers include polyvinylidene fluoride (PVDF), trifluoroethylene, (TrFe), and co-polymers of PVDF and TrFe. Exemplary co-polymers include the PVDF and TrFe in concentrations ranging from 10-90 percent. However, other embodiments may use other concentrations. [Emphasis added.]

Applicant asserts that Agarwal utilizes the ferroelectric effect to save the data in the memory, in contrast to Katoh. Katoh utilizes a completely different effect, described below.

The Examiner states that Agarwal is silent about the distances(s) between the central lines of the word lines and the distance(s) between the central lines of the bit lines. Only for the sake of completeness, Applicant opposes that Agarwal clearly shows in FIG. 4 and 5 that the distance between the centerlines of electrode structures 14, 16 and 18 are the same as between electrode structures 34, 36 and 38.

The Examiner proclaims in the third paragraph of Page 4 of the Office Action that Katoh discloses a memory device, as shown in figs. 1-11, comprising ferroelectric memory cell 52 between bit lines 51 and word lines 50, wherein the distance(s) between the central lines of the bit lines 51 being larger than the distance(s) between the central lines of the word lines 50. The Examiner refers to paragraphs [0015], [0060] and [0072].

Applicant cannot completely agree with the Examiner's statement. In reality, Katoh discloses bit lines (51) and word lines (50) nonparallel to one other which are so arranged as to cross, and a tunneling <u>magneto</u>-resistance element (52) (TMR) used as a memory cell is arranged between a bit line and a word line only at their intersection. The storage device does not exhibit ferro<u>electric</u> memory as alleged by the Examiner. Furthermore, Katoh utilizes the tunnel magneto-resistance based on ferromagnetism. See paragraphs [0046] and [0057] shown on Page 3, column 1 and 2 in Katoh:

> *[0046] The semiconductor storage device of the present embodiment has word lines (W1, W2, W3) 50, bit lines (B1, B2, B3, B4) 51, TMRs (C1) 52, a word line control circuit 53, a bit line control circuit 54, a word line terminating circuit 55, a bit line terminating circuit 56, a distinction circuit 57, a switching circuit 58, and a reference voltage generation circuit 59. In FIG. 1, the bit line B4 is omitted. <u>As shown in FIG. 1, the TMRs 52 are formed in intersecting portions between the word lines 50 and the bit lines 51 as viewed in the plan view.</u> FIG. 4 shows a sectional view of portions of the TMR 52. <u>The TMR 52 is disposed between a lower electrode 105 and an upper electrode 106, and an antiferromagnetic layer 101, a pinned layer 102 (ferromagnetic layer), a tunneling insulating layer 103, and free layer (ferromagnetic layer) 104 are stacked to constitute the TMR.</u> The free layer 104 contacts the upper electrode 106, and the antiferromagnetic layer 101 contacts the lower electrode 105. The upper electrode 106 contacts the word line 50, and may constitute a part of the word line. The lower electrode 105 is connected to the bit line 51, and may constitute a part of the bit line. In this manner, the upper and lower electrodes for the TMR 52, especially the lower electrode may constitute a part of the wiring connected to the electrodes (this also applies to the following embodiments).*
>
> *[0057] Next, a method of using the semiconductor storage device will be described. <u>This semiconductor storage device constitutes a nonvolatile memory in which the TMR is used as a storage element</u>. As shown in FIG. 1, each TMR 52 has a rectangular shape having a long side in a bit line width direction in a plan view, and a <u>magnetized state changes with a current magnetic field of the bit line 51</u> because of this shape anisotropy.*
> [Emphasis added.]

The ferroelectric effect used by Agarwal and the TMR (tunnel magneto resistance) based on ferromagnetism which is used by Katoh are two completely different physical effects, with their own properties and problems. In physics, the ferroelectric effect is an electrical phenomenon whereby certain ionic crystals and piezoelectric polymers may exhibit a spontaneous dipole moment, which can be reversed by the application of an electric field, whereas the TMR occurs when two Ferro magnets are separated by a very thin insulator. Then the resistance of the tunneling current changes with the relative orientation of the two magnetic layers. The resistance is normally higher in the anti-parallel case. Ferromagnetism itself is a phenomenon by which a material can exhibit a spontaneous magnetization.

Thus the cited references from Agarwal and Katoh belong to different technical fields. Applicant has difficulty seeing how the polymer-based ferroelectric memory structure of Agarwal can be combined with the TMR-based semiconductor storage device of Katoh.

Furthermore, Agarwal does not appreciate the underlying problem described by Katoh, because of the different physical effects as described in paragraph [0007] show on page 1, column 2 in Katoh:

> *[0007] Here, integration is considered. As one factor which inhibits the integration, there is a disturbance phenomenon which occurs in performing writing with respect to an adjacent cell. In this phenomenon, data written in the adjacent cell in the magnetized state is collapsed by a magnetic field generated by the wiring in a case where the current is passed through the word line or the bit line to perform the writing with respect to the cell. This phenomenon is influenced by a distance relation between the magnetoresistance element and the wiring to be originally written, and a distance relation between the magnetoresistance element and the adjacent cell. That is, when a pitch between the wirings is smaller, or the distance*

between the magnetoresistance element and write wiring (word line, bit line) is longer, the write wiring of the magnetoresistance element is not easily distinguished from that of an adjacent element, and therefore a possibility of disturbance increases. [...]

The solution Katoh uses to solve this special tunneling magneto-resistance based problem is to use different pitches in the wirings of the first and second systems as described in paragraph [0022] shown on page 2, column 2 in Katoh:

> *[0022] In the present invention described above, in the wirings of the first and second systems, the wiring having a larger distance from the free magnetic layer of the magnetoresistance element is constituted as the bit line or the write bit line which is a wiring having a comparatively large width and arrangement pitch, and the wiring having a smaller distance from the free magnetic layer of the magnetoresistance element is constituted as the word line which is a wiring having a comparatively small width and arrangement pitch, so that disturbance is suppressed, and the arrangement pitch of the word line can be reduced than before. Accordingly, storage cells can be arranged at a high density, and miniaturization and capacity enlargement of the semiconductor storage device are possible by high integration.*

Thus the combination of Katoh's TMR-based semiconductor storage with Agarwal's polymer-based ferroelectric memory is submitted to be improper, because Agarwal teaches away from forming a memory-material-layer with gaps disclosed by Katoh.

Furthermore, the underlying problem is caused by the disturbing magnetic field. Because of the interference between the magnetic fields, Katoh uses different pitches in bit lines and word lines. Agarwal and the Applicant do not appreciate this problem because there are no disturbing magnetic fields in the presence of the ferroelectric effect.

Moreover, the combination could not be made physically because the cited references are from different technical fields. It is impossible to combine the electric-field based memory of Agarwal with the magnetic-field based memory of Katoh. It is impossible to change the state of the electric field of the ferroelectric material described by Agarwal with a magnetic field described by Katoh. Even if they could be combined, it would not work.

Applicant therefore submits that claim 1 is not obvious and should be patentable over the combination of references.

Claims 2-4 depend from claim 1, and should be allowable for at least the same reasons as claim 1.

Claims 5 and 8 include limitations that are similar to claim 1, in the sense that the differential spacing of word lines and bit lines of a polymer memory are claimed. Claims 5 and 8 should thus be allowable for similar reasons as claim 1.

Claims 6 and 7 depend from claim 5, and should be allowable for at least the same reasons as claim 5.

Claims 9 and 10 depend from claim 8, and should be allowable for at least the same reasons as claim 8.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 1-10 under 35 U.S.C. § 103(a) as being obvious over Agarwal in view of Katoh.

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or

assist in the allowance of the present application, the Examiner is invited to call Stephen M. De Klerk at (408) 720-8300.

Please charge any shortages and credit any overages to Deposit Account No. 02-2666. Any necessary extension of time for response not already requested is hereby requested. Please charge any corresponding fee to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Stephen M. De Klerk
Reg. No. 46,503

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300